

# Von Neumann vs Non - Von Neumann: Opposite approaches to algorithm design

Mathematical problem needs an algorithmic solution

Standard (von Neumann) approach

Non- von Neumann approach

Algorithm is designed to match the architecture

Algorithm and architecture are designed jointly

Rigidity of von Neumann architecture makes C algorithm complex and slow



Bottlenecks appear



```
library IEEE;
use IEEE.ALL;
use IEEE.NUMERIC_FIXED_POINT_LITERALS;

entity C_code is
    port(
        clk: in std_logic;
        reset: in std_logic;
        data_in: in integer;
        data_out: out integer;
    );
end entity C_code;

architecture Behavioral of C_code is
    signal register: integer := 0;
begin
    process (clk, reset)
    begin
        if reset = '1' then
            register <= 0;
        else
            register <= data_in;
        end if;
        data_out <= register;
    end process;
end architecture Behavioral;
```

Compilation

Slow execution



Development tool is a PC or high-performance computer

Since the architecture is developed jointly with the algorithm, the design process is smooth and natural. Speed-up factors on the order of 1,000 are achievable (when compared against Von Neumann algorithms).

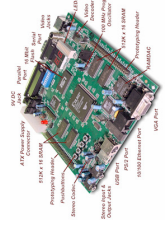
VHDL Code

```
library IEEE;
use IEEE.ALL;
use IEEE.NUMERIC_FIXED_POINT_LITERALS;

entity VHDL_code is
    port(
        clk: in std_logic;
        reset: in std_logic;
        data_in: in integer;
        data_out: out integer;
    );
end entity VHDL_code;

architecture Behavioral of VHDL_code is
    signal register: integer := 0;
begin
    process (clk, reset)
    begin
        if reset = '1' then
            register <= 0;
        else
            register <= data_in;
        end if;
        data_out <= register;
    end process;
end architecture Behavioral;
```

Synthesis



Programming language is VHDL



Development tool is a commercially available FPGA board. Cost is comparable to that of a PC.