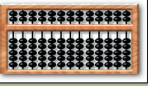






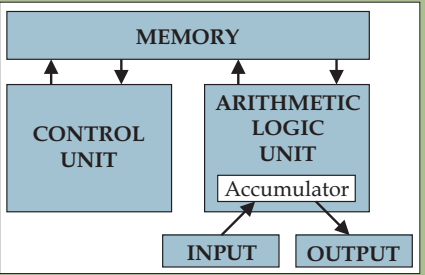


Algorithm Development: From Euclid's "Elements" to the latest breakthroughs in jointly designed algorithms / machine-architectures

Algorithms & Machines milestones through history

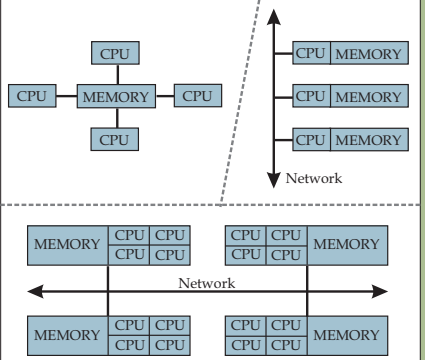
Algorithm	Machine
Early algorithm and machine developments: Machine and Algorithm were considered independent problems	
350 B.C. "Elements"; Greatest Common Divisor Algorithm <i>Euclid</i>	
780 - 850 Works on arithmetic and algebra <i>Al-Khwarizmi</i>	1200 Abacus <i>Chinese</i> 
1669 Newton's method (gradient methods) <i>Isaac Newton</i>	1642 - 1645 Pascalene <i>Blaise Pascal</i> 
1797 Lagrange multipliers (constrained optimization) <i>Joseph-Louis Lagrange</i>	
1947 Simplex algorithm (linear programming) <i>G. B. Dantzig</i>	1945 von Neumann Architecture <i>John von Neumann</i> 
1971 Sequential branch and bound algorithms (global optimization) <i>Piyavskii-Shubert</i>	
1984 Interior point methods (large-scale linear programming) <i>Karmakar</i>	
Increased sophistication in machines led to specialized algorithms designed for the machine	
1965 Cooley-Tukey parallel FFT algorithm <i>John W. Tukey</i>	1950 First parallel computer <i>Svoboda</i> 
1987 - today Parallel branch and bound algorithms	1977 ARCnet - First clustering product <i>Datapoint</i> 
1990 - today Parallel interior point methods	
1994 - today Grid computing algorithms for branch and bound	1997 dnet - First distributed computer network (Grid computing) 
Recent advances in reconfigurable computing allow the joint design of algorithm and machine architecture	
	2005 Accelelogic demonstrates the world's first custom-computing solution for large-scale optimization (joint design of algorithm and machine architecture enable historic speed ups) <i>Accelelogic</i>

Sequential Algorithms → von Neumann Architecture



Potential Issues	Speed-up Factor
von Neumann bottleneck Extremely serious	1
Scalability Very limited	
Capacity Low	
Cost Very inexpensive	

Distributed Algorithm → Network Cluster Architecture



Potential Issues	Speed-up Factor
von Neumann bottleneck Extremely serious	Up to N
Scalability Problem dependent	
Capacity Problem dependent	
Cost Very expensive	

Jointly Designed Algorithm / Architecture

Algorithm and architecture are designed jointly


VHDL Code

```

library IEEE;
use IEEE.ALL;
use IEEE.STD_LOGIC.ALL;

process (clk_in, reset)
begin
    if ( reset = '0' ) then
        diffregister <= '000';
        clk_in <= reset;
    else
        diffregister <= muxout;
        and fcs;
    end process;
    
```

Synthesis



Since the architecture is developed jointly with the algorithm, the design process is smooth and natural. Speed-up factors of up to 100,000 are achievable (when compared against von Neumann algorithms).

Programming language is VHDL

Development tool is a commercially available FPGA board. Cost is comparable to that of a personal computer.

Potential Issues	Speed-up Factor
von Neumann bottleneck Not present	Up to 100,000
Scalability Almost linear	
Capacity Very large	
Cost Problem dependent	

