accelogic
Redefining Algorithm R&D

Training Series on HPC with Reconfigurable Computing

Algorithm Design in the Era of Reconfigurable Computing

Dates: To be announced
Place: To be announced
Price: Early registration: $1,490
Late registration: $1,750

Course Description:

The astonishing developments seen in the field of reconfigurable computing during the last five years, bring an unprecedented opportunity for the acceleration of complex computations in science and engineering applications. Reconfigurable computing algorithms implemented in FPGAs are often 10x to 1,000x faster than traditional parallel algorithms, and can usually be developed for a fraction of the cost of a supercomputer or computer cluster solution.

Many high-performance computing applications are turning to FPGAs and reconfigurable computing to squeeze performance for their biggest computational challenges. FPGAs are becoming a commodity in computational science – even traditional non-FPGA companies like SGI and Cray are incorporating FPGAs into their latest supercomputers, as the *de facto* platform for the removal of computational bottlenecks.

Besides the fact that reconfigurable computing is reaching maturity as a robust technology for high-performance computing, there are still relatively few people who understand it deeply enough to be able to do cutting-edge algorithm research or develop

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serious industrial applications with it. Reconfigurable computing is creating a deep "knowledge-divide" that separates those who can and cannot work well with it. Those who understand it and know how to exploit it to the fullest, are leading the way in research innovations and are winning the race in the development of new and more powerful industrial applications.

The purpose of Accelogic's *Training Series on HPC with Reconfigurable Computing* is to contribute to the dissipation of this knowledge-divide in the vast variety of fields where faster numerical computation is a key driver for industrial development and scientific innovation. This course is intended as a thorough initial exposure to reconfigurable computing for algorithm developers and scientists who have never worked with FPGAs. The emphasis is on algorithms and the concepts behind good design – concepts which often cannot be found in academic textbooks and are rather guarded as "tricks of trade" by industry. The target audience is made of professionals in any field where faster algorithms means better products, better design processes, or better chances to answer new research questions. This includes fields like computational mechanics, aerospace engineering, financial engineering, operations research, drug discovery, computational linguistics, numerical analysis, electronic chip design, automotive design, computational electromagnetics and computational chemistry among many others.

Although the algorithm implementation cycle in reconfigurable computing is similar in principle to that of a traditional software solution (code a program, debug, compile, test), mastering the art of reconfigurable computing requires a paradigm shift in the thought process of the algorithm developer. This course walks you through that paradigm shift, from an essentially sequential way of thinking (i.e., instruction-based software), into a world where numerical manipulation is as free and creative (and eventually fun too!) as playing Lego design.

Under this new paradigm, you free yourself from the limitations imposed by an instruction-based machine architecture (known in the literature as the "von Neumann or software bottleneck"), and open the door to a liberated world, full of opportunities for the discovery of new and groundbreaking algorithms, in which you can manipulate the machine architecture to best solve your problem (i.e., you design jointly the algorithm and the architecture).

While walking you through these new concepts, the course introduces you to the basics of FPGA-based development, the VHDL programming language, compiling, debugging, and synthesis tools. Five hands-on sessions ensure your direct exposure to the complete algorithm design process, from conception and design, to coding, debugging, compiling, testing, and using the algorithm in a real reconfigurable computing platform.

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By the End of the Course…

By the end of the course, you will have a thorough understanding of the enormous benefits that FPGAs and reconfigurable computing can bring to the resolution of difficult numerical problems, and will have a firm grasp of the process necessary to bring an algorithm from conception to use in a reconfigurable computing platform.

You will also have a clear idea of the concepts behind good reconfigurable computing design, and will have developed criteria to compare the potential performance gains of reconfigurable computing vs. traditional software-oriented algorithms in practical applications.

Finally, you will be armed with the necessary knowledge to design simple accelerated algorithms under this new paradigm, and implement them in a practical reconfigurable computing platform.

Course Contents:

DAY 1

Session 1: Introduction to reconfigurable computing

Introductory talk giving a broad description of the reconfigurable computing concept. Topics of the session include:

- What is reconfigurable computing?
- From the early logic devices to the era of programmable logic
- Von Neumann computer architectures
- Software bottleneck
- Design styles: the software paradigm, the hardware paradigm, and the configurable hardware paradigm.
- Hardware technologies: ASIC, PAL, PLD, FPGA
- Advantages of reconfigurable computing
- Challenges in reconfigurable computing

Session 2: The ABC of reconfigurable computing

Lecture on the common terms and jargon of reconfigurable computing:

- Combinational circuit
- Sequential circuit
- Memory

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- State machine
- Concurrent design
- Signal
- Simulation vs synthesis
- Entity, port, architecture, driver, delay, etc.

Session 3: Design tools (HANDS-ON)

A quick overview of the basic tools for algorithm design with reconfigurable computing. It includes software tools for FPGA development, as well as a discussion on the key players in the market and their offerings.

- The hardware:
  - FPGAs
  - Memory
  - Development boards
  - Specialized boards
  - Lab equipment
- The software:
  - Hardware description languages
  - Design capture (schematics, HDL)
  - Design validation (simulation)
  - Physical design (synthesis)
  - High level tools: C to HDL "wizards" (pros and cons)

Session 4: The design process flow (HANDS-ON)

Practical session where, based on code provided by the instructor, the student goes step by step through the design process flow:

- Coding
- Simulation
- Synthesis
- Verification
- Programming of the device

DAY 2

Session 5: Manipulating numbers inside an architecture

Lecture on the different ways to represent the components and interconnection of numerical operations:

- Structural (bit) level

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- Register Transfer level (RTL)
- Algorithmic level
- Finite state machines and datapaths
- Adders and multipliers
- Transcendental functions
- Example: fixed point vs. floating point arithmetic inside an algorithmic solution

Session 6: VHDL basics, part 1

This session introduces the basic concepts of the VHDL programming language, the de-facto standard for reconfigurable computing programming.

- Basic structures in VHDL
- Types
- Operators
- Sequential statements

Session 7: Designing an algorithm in VHDL (HANDS-ON)

Practical session where the student needs to design and simulate a solution for a toy problem.

- Understanding the problem.
- Identifying advantages of reconfigurable computing compared against conventional von Neumann solutions for the problem to solve.
- Designing the solution: schematics.
- Describing the solution: from schematics to VHDL code.
- Simulation of the VHDL design.

Session 8: Implementing an algorithm in an FPGA (HANDS-ON)

Practical session that, based on the design of session 7, covers the concepts behind the physical programming of an FPGA.

- Synthesis
- Post-synthesis simulation
- Programming the FPGA
- Running the program

DAY 3

Session 9: VHDL basics, part 2

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This lecture is the continuation of session 8. Topics include:

- Concurrent statements
- Subprograms and packages
- Optimization of the code

Session 10: Designing efficient algorithms

Introduction of important concepts and practices for industrial-quality reconfigurable computing algorithm design.

- Using minimum bit width
- Sharing complex operators
- Parallelization (in time –pipelining- and space –replication-)
- Interface with host computers

Session 11: Design and implementation of a practical algorithm (HANDS-ON)

This module is a practical session where the goal is to develop a simple but practical solution to an algorithmic problem using the reconfigurable computing paradigm. The problem is chosen according to the particular interests of the students.

Session 12: What's next?

Summarizes the main concepts behind reconfigurable computing, and gives an indication of the future of the technology in the context of high-performance computing.

- Advantages of reconfigurable computing in HPC
- Trends and challenges of reconfigurable computing
- Further training: VHDL Programming, Advanced Algorithm Design, …
- Specialized courses: Finite Elements, CFD, Numerical Linear Algebra, MDO, Finance, Computational Linguistics, …

Lab Equipment:

The use of all laboratory and computer equipment is included in the course fee. Equipment includes:

- IBM PC or compatible, running Windows Vista, XP, Windows 2000 w/SP2.
- Software licenses for design, synthesis, verification, and programming of FPGA hardware devices (Xilinx ISE).
- Evaluation boards (Xilinx Spartan-3 LC Development Kit DS-KIT-3SLC400 or similar).

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Registration and additional information:

Registration/participation is limited and available on a first-come, first-served basis. Register by emailing a complete registration form to training@accelogic.com or faxing it to Accelogic at (954) 208-0018. We accept credit cards (Visa, MasterCard, or American Express) as well as company or Government purchase orders. Accelogic offers a money-back satisfaction guarantee on all of its courses.

For more information please contact Ms. April Sortor at april.sortor@accelogic.com, or call (954)888-4711.

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Course Registration Form

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